

DESCRIPTION

AMCOM's AM003536WM-BM/FM-R is an ultra broadband GaAs MMIC power amplifier. It has 23 dB gain, and 36 dBm output power over the 0.01 to 3.5 GHz band. This MMIC is in a ceramic package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. AM003536WM-FM-R is AM003536WM-BM-R assembled on a copper flange carrier for screwing on to a metal heat sink. Both parts are RoHS compliant.

FEATURES

- Wide bandwidth from 10MHz to 3.5 GHz
- High output power, P1dB = 36 dBm
- High gain, 23dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: $V_{dd} = +20V$, $I_{dq1} = 150mA$, $I_{dq2} = 550mA$)

Parameters	Minimum	Typical **	Maximum
Frequency	0.02 – 2.5GHz	0.01 – 3.5GHz	-
Small Signal Gain	20 dB	23 dB	26 dB
Gain Ripple	-	± 1.5 dB	± 3.0 dB
P1dB @ 1 GHz	33.0 dBm	35.0 dBm	-
Psat	35.0 dBm	37.0 dBm	-
Efficiency @ P1dB	-	20 %	
IP3 @ 1GHz	-	48 dBm	
Input Return Loss	13 dB	20dB	
Output Return Loss	7 dB	10dB	
Thermal Resistance		4.5 °C/W	

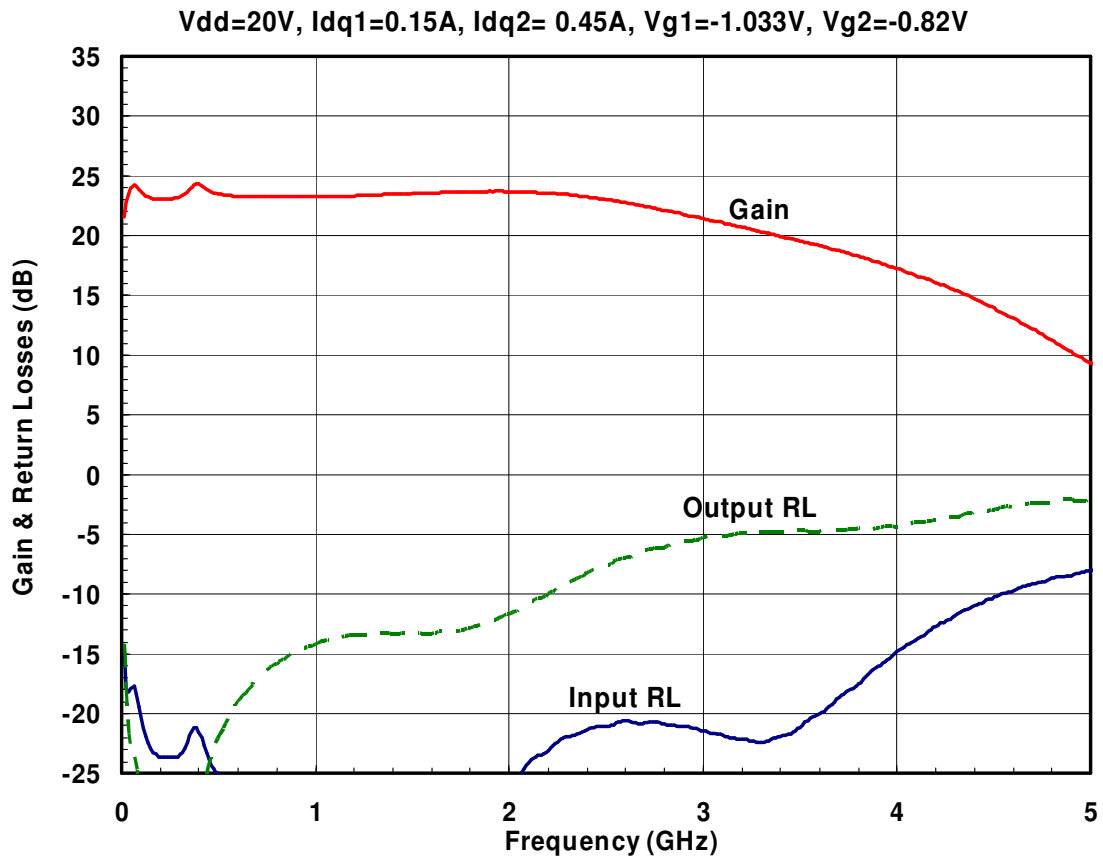
* Specifications subject to change without notice.

** Gate biases corresponding to above currents are $V_{gs1} = -1V$, $I_{gs1} < 2mA$, $V_{gs2} = -0.75V$, $I_{gs2} < 5mA$ and may vary from lot to lot. Gate currents could reach above limits only near power saturation

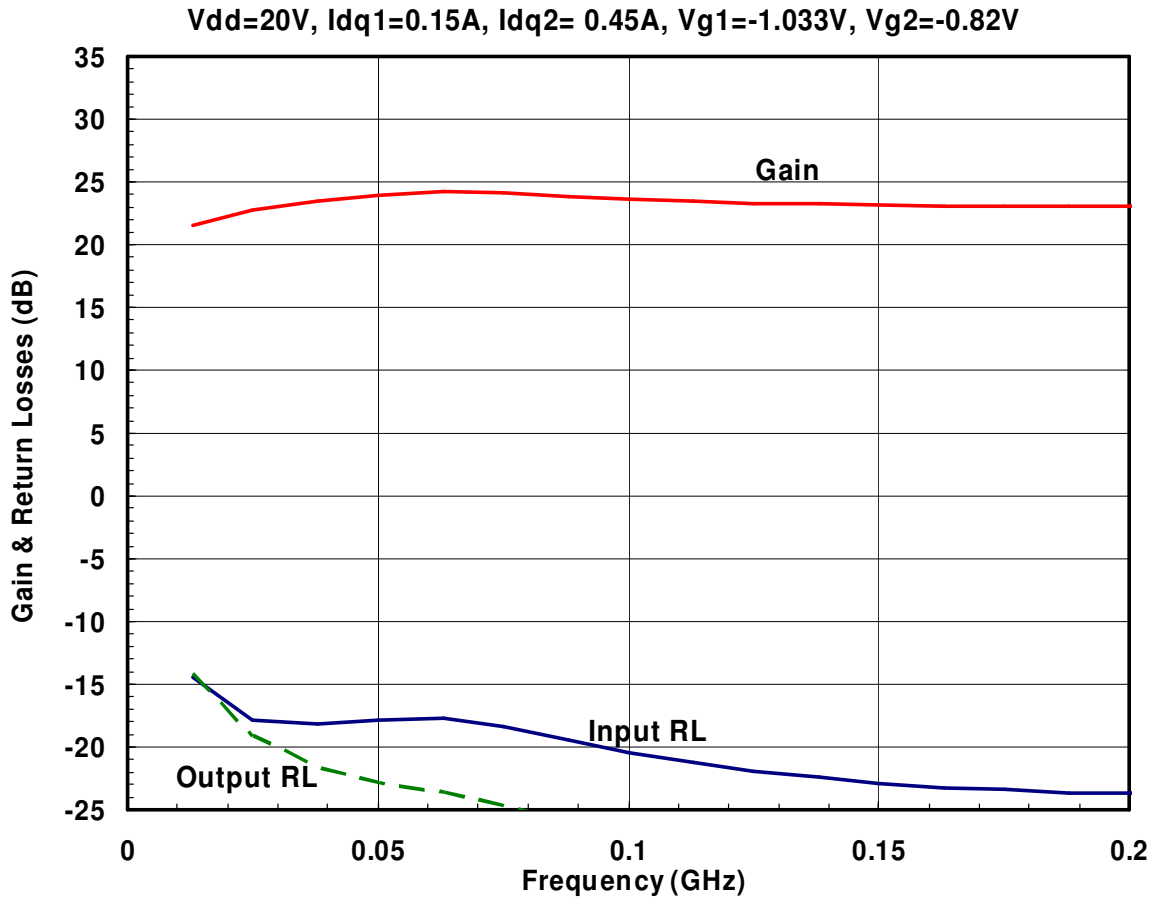
ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating
Drain source voltage	V_{dd}	24 V
Gate source voltage	V_{gs1} & V_{gs2}	-3 V
Drain source current	I_{dq1}	0.17 A
Drain source current	I_{dq2}	0.60 A
Continuous dissipation at 25°C	P_t	18 W
Channel temperature	T_{ch}	175 °C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

SMALL SIGNAL DATA*

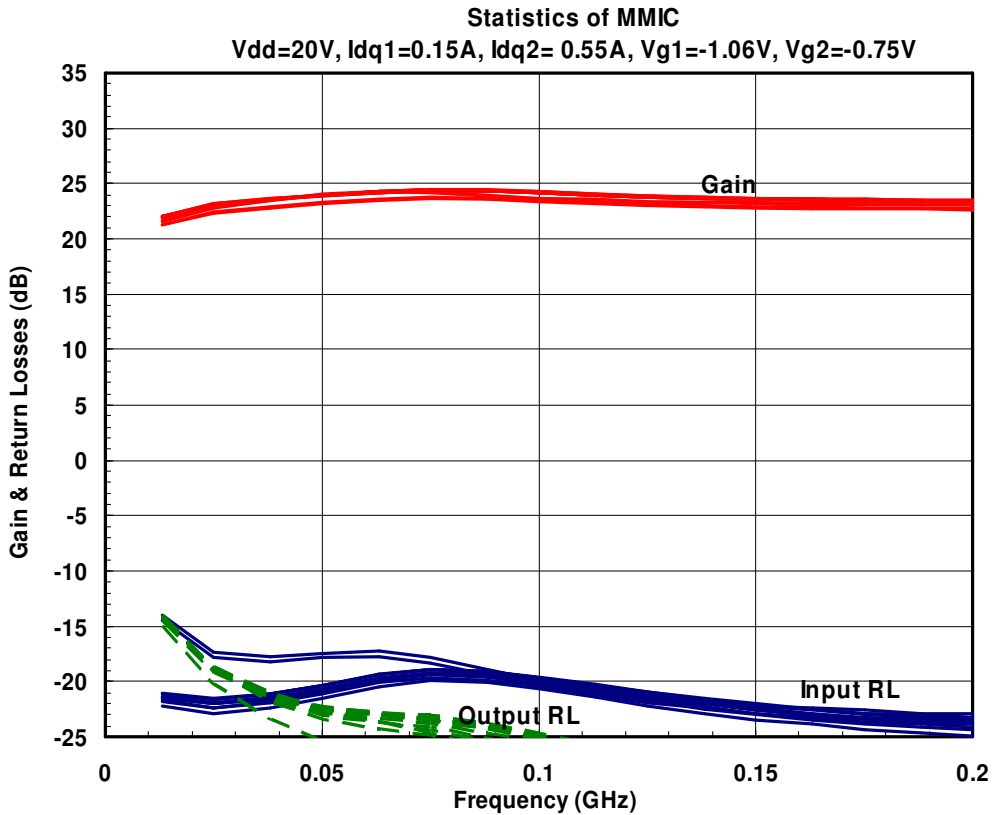
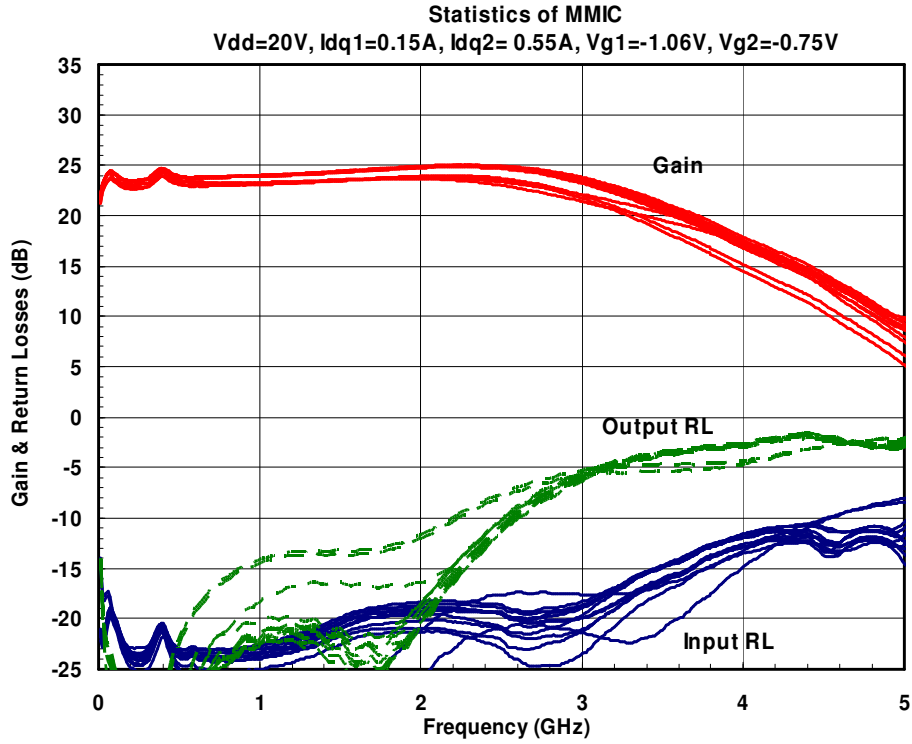


EXTENDED LOW FREQUENCY SCALE

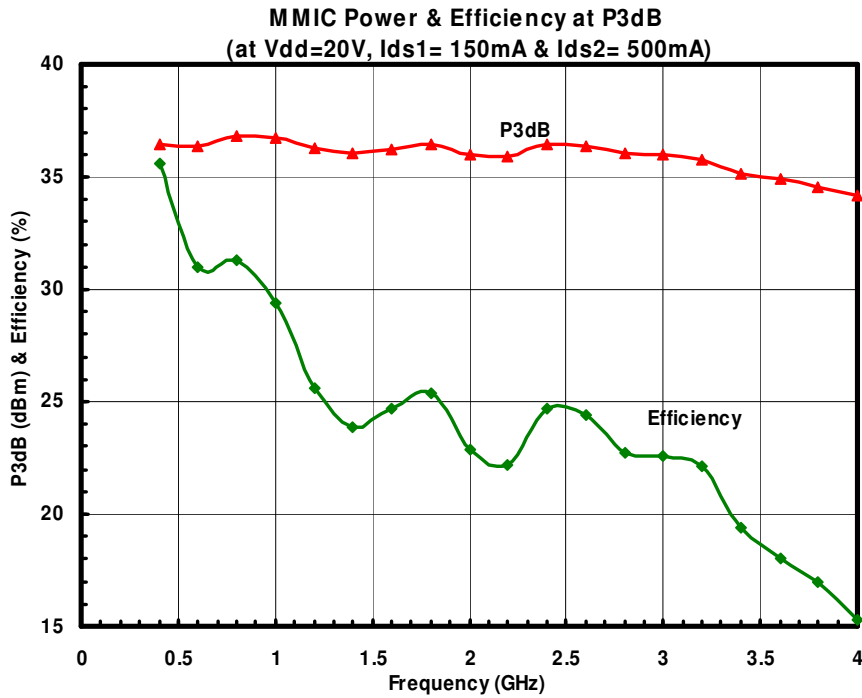
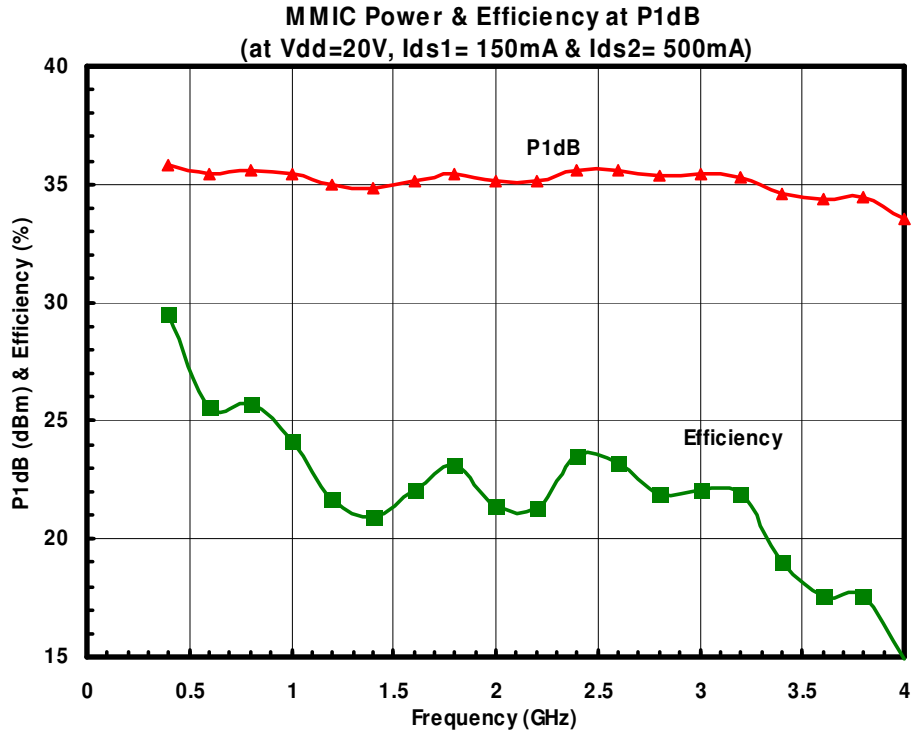


* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than $V_{dd}=+20V$ with almost same small signal parameters. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments

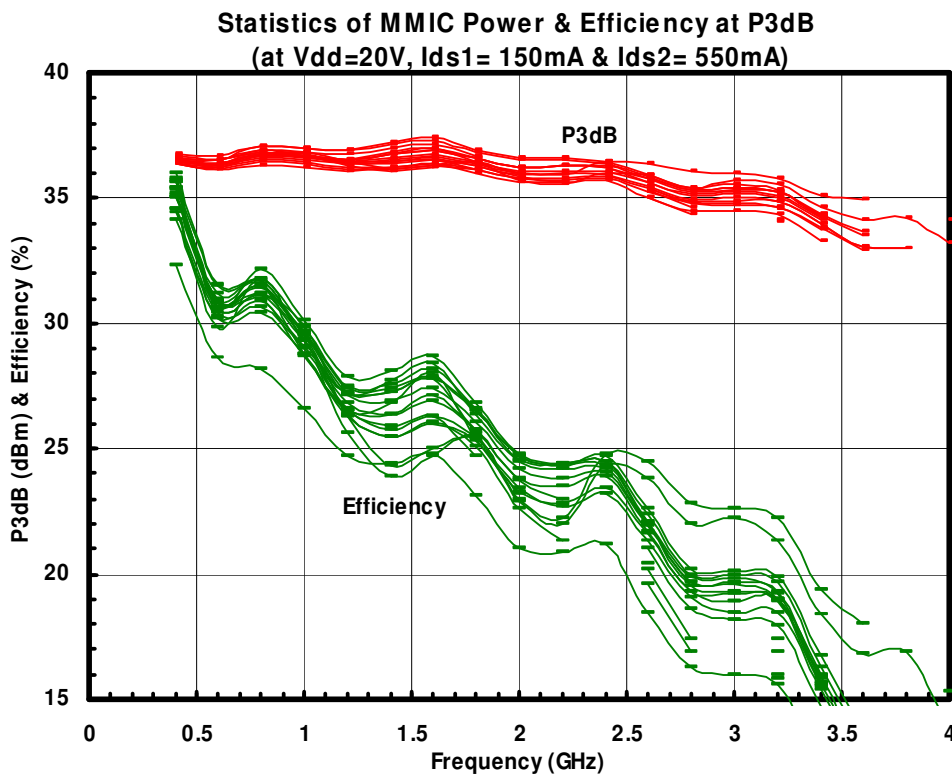
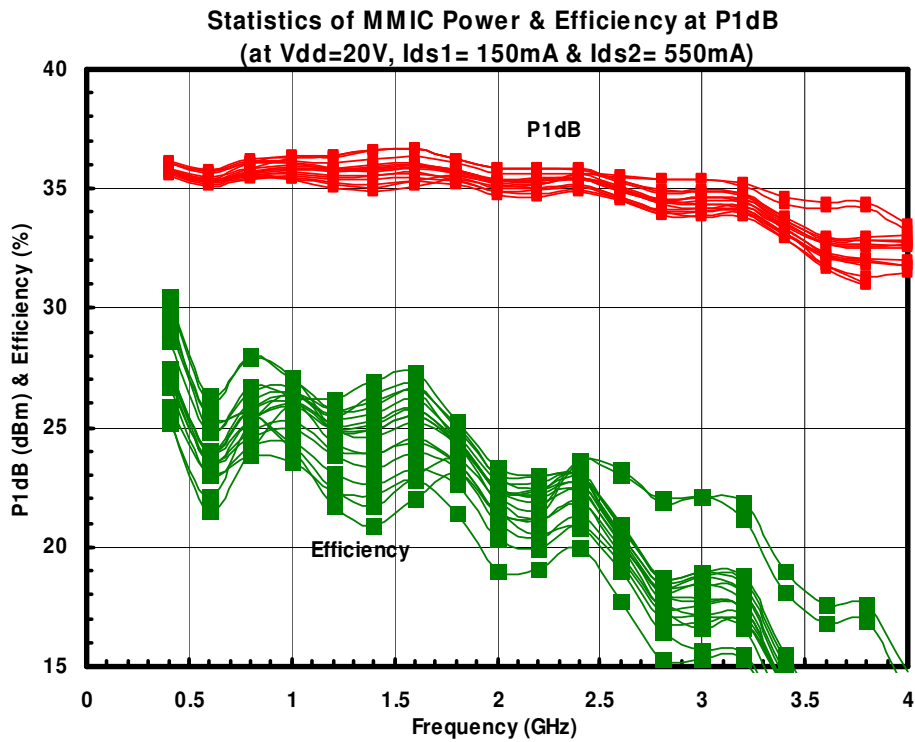
SMALL SIGNAL STATISTICS



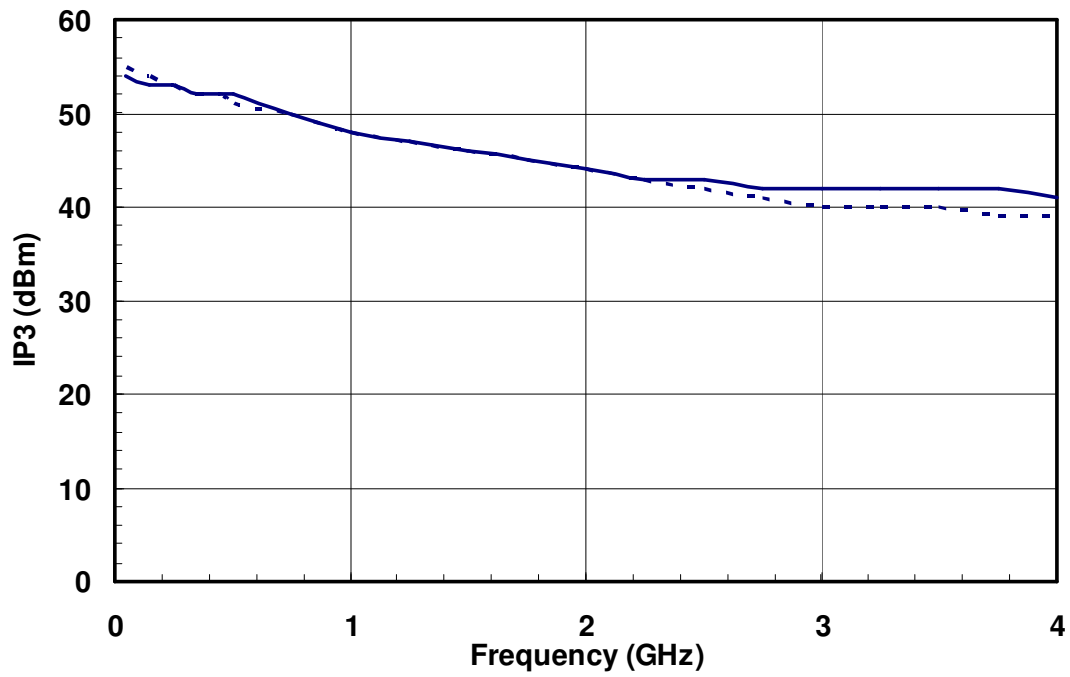
POWER DATA*



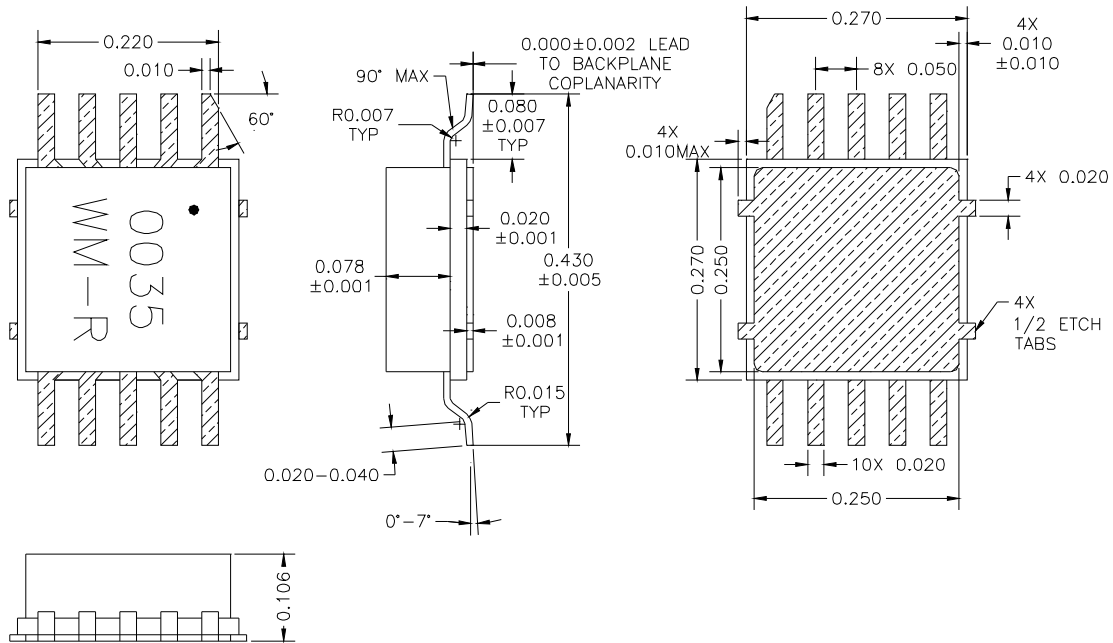
* Power measured using bias tee at the output. MMIC could be operated at lower than $V_{dd}=+20V$ with reduced power output. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments



IP3 as a function of Frequency

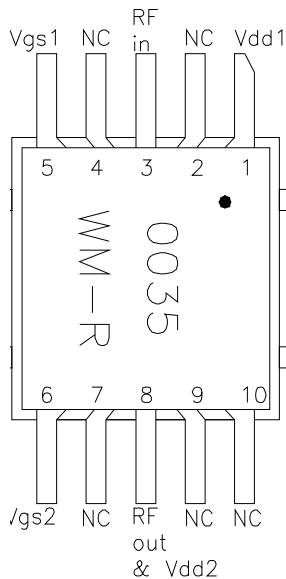


PACKAGE OUTLINE (BM)



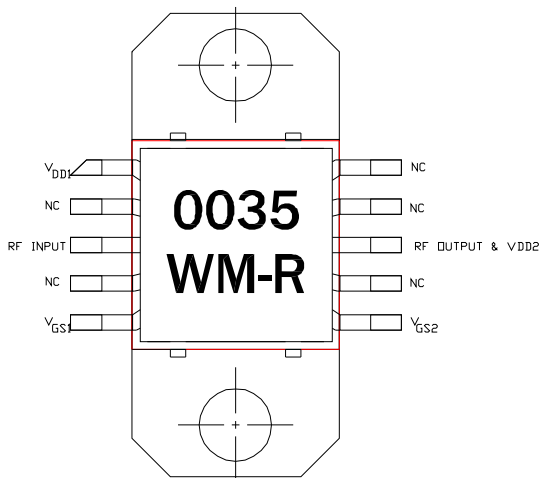
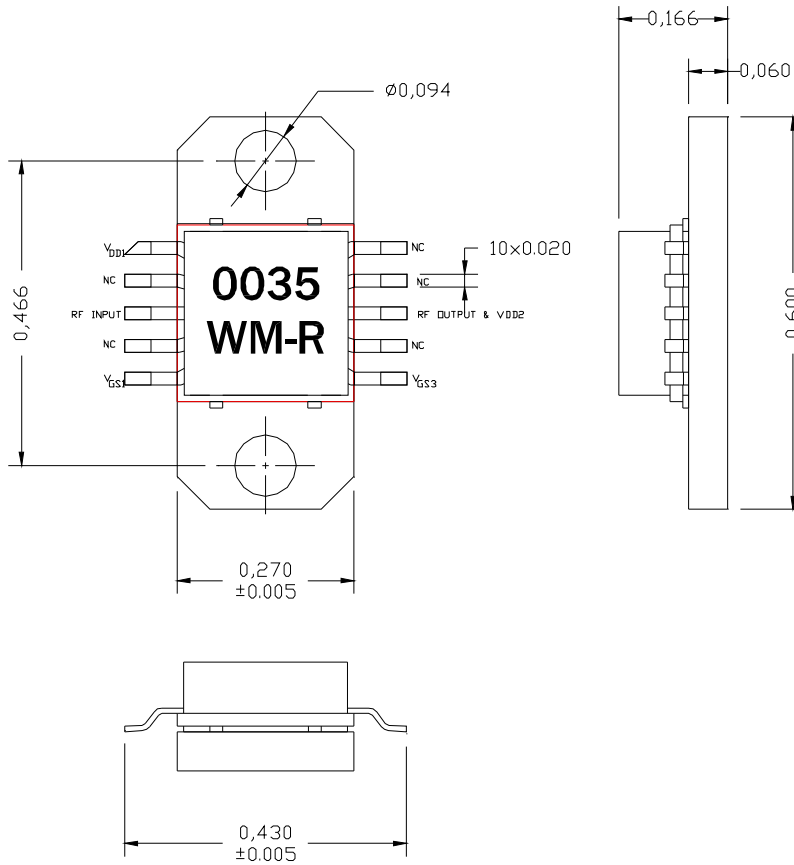
* Gate biases are for reference only and may vary from lot to lot

Pin Layout



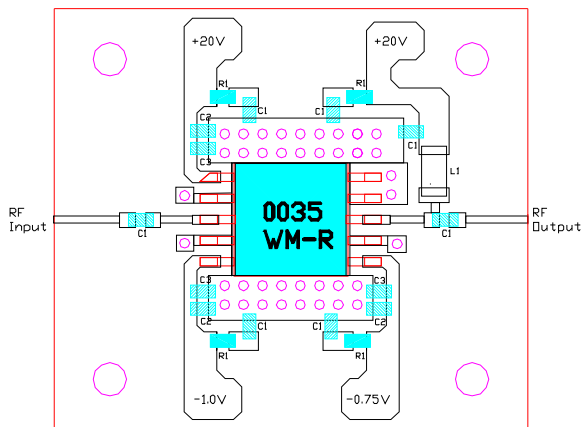
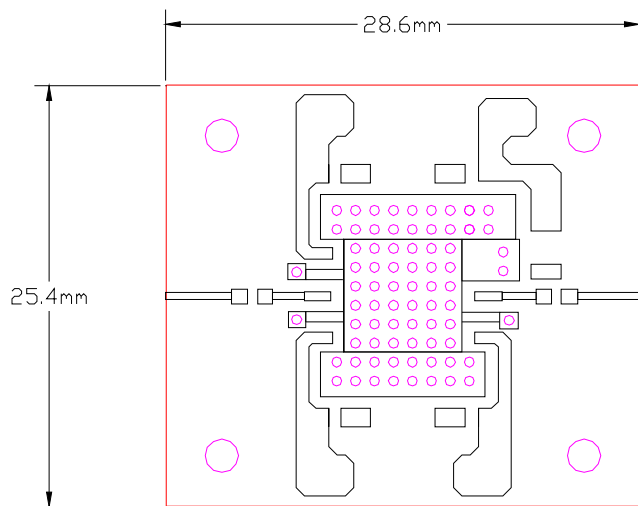
Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.0V
6	Vgs2	-0.75V
7	NC	
8	Vdd2 & RF out	+20V
9	NC	
10	NC	

PACKAGE OUTLINE (FM)



Pin No.	Function	Bias
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.0V
6	Vgs2	-0.75V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

Pin Layout

TEST CIRCUIT for BM Package**Notes:**

- 1- Material is 10mils FR4 with 1 Oz Copper
- 2- All vias are plated thru (min. via thickness = 25um)
- 3- R1=500hms, R2=00hms,
C1=1000pF, C2=100pF, C3=20pF, L1=300nH
- 4- Bias could be supplied to the RF output port using a bias tee.

Resistor
 Capacitor

Important Notes:

- 1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).
- 2- Recommended current biases are 150mA and 500mA for the first stage and second stage respectively. Gate biases are for reference only. At V_{dd1} & $V_{dd2} = +20V$, V_{gs1} & V_{gs2} values are -1.0V and -0.75V respectively to obtain these desired currents. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.
- 3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2} .
- 4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 2mA & 5mA respectively at P_{1dB} .